What is claimed is:

1. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate and having a plurality of integrated circuit devices, wherein the integrated circuit is formed by a method comprising:

depositing a conductive layer above an insulating material;

patterning the conductive layer to form a plurality of first metal features and at least one second metal feature, wherein

the first metal features and the at least one second metal feature have a substantially equal thickness, T_{met}, above the insulating material, and

the first metal features have a substantially standard distance, S_{met}, between parallel edges of adjacent ones of the first metal features, and

the at least one second metal feature is connected to one or more of the first metal features in proximity to an intersection area of the conductive layer,

wherein an intersection area is a roughly rectangular area that includes at least one metal feature corner, parts of at least one other metal feature that are in close proximity to the at least one metal feature corner, and a portion of a dielectric layer that will be located between the at least one metal feature corner and the parts of the at least one other metal feature; and

depositing the dielectric layer having a thickness, T_{IDL}, over the conductive layer.

2. The semiconductor die of claim 1, wherein the insulating material defines a top surface of the integrated circuit devices.

3. The semiconductor die of claim 1, wherein at least some of the integrated circuit devices are memory cells.

4. The semiconductor die of claim 3, wherein the memory cells are Dynamic Random Access Memory (DRAM) memory cells.

5. The semiconductor die of claim 1, wherein patterning the conductive layer comprises performing a photolithography process and a reactive ion etching process.

6. The semiconductor die of claim 1, wherein patterning the conductive layer comprises patterning the at least one second metal feature so that a distance between the at least one second metal feature and another metal feature is less than S_{met}.

7. The semiconductor die of claim 1, wherein the plurality of first metal features includes a plurality of electrically unisolated metal lines, wherein at least three of the electrically unisolated metal lines are substantially parallel.

8. The semiconductor die of claim 7, wherein the plurality of first metal features further includes a plurality of electrically isolated metal features, which function to provide the substantially standard distance between the parallel edges of the first metal features.

9. The semiconductor die of claim 1, wherein an altitude of the dielectric layer above the insulating material roughly equals $T_{met} + T_{IDL}$ over a metal feature, and

the at least one second metal feature maintains an altitude of a portion of the dielectric layer that overlies the intersection area to roughly $T_{met} + T_{IDL}$.

10. The semiconductor die of claim 1, wherein a top surface of the dielectric layer is substantially self-planarized upon depositing the dielectric layer.

11. A memory device, comprising:
an array of memory cells that includes:
one or more memory cells, each with a transistor and a capacitive structure;
a patterned conductive layer deposited above the one or more memory cells and on a top surface of an insulating material, wherein the patterned conductive layer includes a plurality of first metal features and at least one second metal feature, wherein
the first metal features and the at least one second metal feature have a substantially equal thickness, T_{met}, above the insulating material, and
the first metal features have a substantially standard distance, S_{met}, between parallel edges of adjacent ones of the first metal features, and
the at least one second metal feature is connected to one or more of the first metal features in proximity to an intersection area of the conductive layer,
wherein an intersection area is a roughly rectangular area that includes at least one metal feature corner, parts of at least one other metal feature that are in close proximity to the at least one metal feature corner, and a portion of a dielectric layer that will be located between the at least one metal feature

corner and the parts of the at least one other metal feature; and

a dielectric layer deposited over the patterned conductive layer, wherein the dielectric layer has a thickness, T_{IDL}, above the patterned conductive layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

12. The memory device of claim 11, wherein the one or more memory cells are Dynamic Random Access Memory (DRAM) memory cells.

13. The memory device of claim 11, wherein a distance between the at least one second metal feature and another metal feature is less than S_{met}.

14. The memory device of claim 11, wherein the plurality of first metal features includes a plurality of electrically unisolated metal lines, wherein at least three of the electrically unisolated metal lines are substantially parallel.

15. The memory device of claim 11, wherein the plurality of first metal features further includes a plurality of electrically isolated metal features, which function to provide the substantially standard distance between the parallel edges of the first metal features.

16. The memory device of claim 11, wherein an altitude of the dielectric layer above the insulating material roughly equals $T_{met} + T_{IDL}$ over a metal feature, and the at least one second metal feature maintains an altitude of a portion of the dielectric layer that overlies the intersection area to roughly $T_{met} + T_{IDL}$.

17. The memory device of claim 11, wherein a top surface of the dielectric layer is substantially self-planarized upon depositing the dielectric layer.

18. An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

a substrate; and

an integrated circuit supported by the substrate and having a plurality of integrated circuit devices, wherein the integrated circuit is formed by a method comprising:

depositing a conductive layer above an insulating material;

patterning the conductive layer to form a plurality of first metal features and at least one second metal feature, wherein

the first metal features and the at least one second metal feature have a substantially equal thickness, T_{met}, above the insulating material, and

the first metal features have a substantially standard distance, S_{met}, between parallel edges of adjacent ones of the first metal features, and

the at least one second metal feature is connected to one or more of the first metal features in proximity to an intersection area of the conductive layer,

wherein an intersection area is a roughly rectangular area that includes at least one metal feature corner, parts of at least one other metal feature that are in close proximity to the at least one metal feature corner, and a portion of a dielectric layer that will

be located between the at least one metal feature corner and the parts of the at least one other metal feature; and

depositing the dielectric layer having a thickness, T_{IDL}, over the conductive layer.

19. The electronic system of claim 18, wherein the insulating material defines a top surface of the integrated circuit devices.

20. The electronic system of claim 18, wherein at least some of the integrated circuit devices are memory cells.

21. The electronic system of claim 20, wherein the memory cells are Dynamic Random Access Memory (DRAM) memory cells.

22. The electronic system of claim 18, wherein patterning the conductive layer comprises performing a photolithography process and a reactive ion etching process.

23. The electronic system of claim 18, wherein patterning the conductive layer comprises patterning the at least one second metal feature so that a distance between the at least one second metal feature and another metal feature is less than S_{met}.

24. The electronic system of claim 18, wherein the plurality of first metal features includes a plurality of electrically unisolated metal lines, wherein at least three of the electrically unisolated metal lines are substantially parallel.

25. The electronic system of claim 24, wherein the plurality of first metal features further includes a plurality of electrically isolated metal features, which function to provide the substantially standard distance between the parallel edges of the first metal features.

26. The electronic system of claim 18, wherein an altitude of the dielectric layer above the insulating material roughly equals $T_{met} + T_{IDL}$ over a metal feature, and the at least one second metal feature maintains an altitude of a portion of the dielectric layer that overlies the intersection area to roughly $T_{met} + T_{IDL}$.

27. The electronic system of claim 18, wherein a top surface of the dielectric layer is substantially self-planarized upon depositing the dielectric layer.